

(19)



JAPANESE PATENT OFFICE

PATENT ABSTRACTS OF JAPAN

(11) Publication number: **04099328 A**

(43) Date of publication of application: **31.03.92**

(51) Int. Cl. **H01L 21/331**
H01L 29/73

(21) Application number: **02217695**

(71) Applicant: **NEC CORP**

(22) Date of filing: **18.08.90**

(72) Inventor: **KONDO MASAKI**

(54) **BIPOLAR TRANSISTOR**

P-type base region 2B.

(57) Abstract:

COPYRIGHT: (C)1992,JPO&Japio

PURPOSE: To prevent current gain from being reduced by allowing impurities concentration distribution of a base region to have two or more peaks and enabling peak concentration to be higher as the depth from a surface is deeper.

CONSTITUTION: In impurities distribution of an NPN type bipolar transistor, 1 and 2 indicate an N-type emitter region with a surface concentration of 10^{20} - 10^{21}cm^{-3} and a P-type base region. This P-type base region 2 consists of a low-concentration base region 2A with a peak concentration of 2×10^{16} - $1 \times 10^{17}\text{cm}^{-3}$ and a high-concentration P-type base region 2B with a peak concentration of 1×10^{18} - $5 \times 10^{18}\text{cm}^{-3}$. Since junction is formed between the low-concentration P-type base region 2A and the N-type emitter region 1 according to this NPN-type bipolar transistor, electric field within a depletion layer is relaxed when voltage is applied in opposite direction and generation of hot carriers can be suppressed. On the other hand, punch through or current gain control can be performed at the high-concentration

